

1 Amendments to the Claims:

2 This listing of claims will replace all prior versions, and  
3 listings, of claims in the application:  
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5 Listing of Claims:

6 1. (Original) A symbol timing synchronizer for generating a timing  
7 signal from a sampled input signal being a received input signal  
8 sampled at a rate of the timing signal, the received input signal  
9 being a continuous phase modulated signal modulated by a symbol  
10 sequence generated from a precoded data sequence of an input data  
11 sequence, sampled input signal having a sampled inphase component  
12 and a sampled quadrature component, the symbol timing synchronizer  
13 comprising,

14 an inphase isolator and a quadrature isolator for respectively  
15 isolating the sampled inphase component and sampled quadrature  
16 component of the sampled input signal for respectively providing an  
17 inphase signal and a quadrature signal,

18 an inphase serial data demodulator and a quadrature serial  
19 data demodulator for respectively receiving and filtering the  
20 inphase signal and the quadrature signal for generating an odd  
21 filter response and an even filter response, and for converting and  
22 sampling the odd and even filter responses into odd data and even  
23 data, the odd data and the even data alternately forming an  
24 estimate of the input data sequence,

25 an inphase error magnitude generator and a quadrature error  
26 magnitude generator for receiving and filtering the inphase signal  
27 and the quadrature signal, for respectively generating and sampling  
28 an inphase error magnitude signal and quadrature error magnitude

1 signal for respectively generating a sampled inphase error  
2 magnitude signal and a sampled quadrature error magnitude signal,  
3 an inphase mixer and a quadrature mixer for respectively  
4 mixing the sampled inphase error magnitude signal with the odd data  
5 into an odd error signal, and mixing the quadrature error magnitude  
6 signal with the even data for generating an even error signal, the  
7 odd data representing an odd sign of the inphase magnitude error  
8 signal, the even data representing an even sign of the quadrature  
9 magnitude signal, and

10 an oscillator means for generating the timing signal from the  
11 even error signal and the odd error signal, the timing signal for  
12 controlling the sampling of the inphase serial data demodulator and  
13 the quadrature serial data demodulator and for controlling the  
14 sampling of inphase error magnitude generator and a quadrature  
15 error magnitude generator for generating the timing signal at a  
16 rate of the symbol sequence.

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19 2. (Original) The symbol timing synchronizer of claim 1 wherein the  
20 oscillator means comprises,

21 a loop filter for receiving the odd error signal and the even  
22 error signal for providing a filter error signal,

23 a controlled oscillator for receiving the filter error signal  
24 for generating the timing signal, and

25 a modulo counter for providing an odd timing signal for  
26 sampling the inphase magnitude error signal, and for providing an  
27 even timing signal for sampling the quadrature magnitude error  
28 signal.

1 3. (Original) The symbol timing synchronizer of claim 1 wherein,  
2 the inphase magnitude error generator generates the inphase  
3 magnitude error signal from a difference between a filter response  
4 of the inphase signal and an odd modulo count of the timing signal,  
5 the inphase magnitude error generator serving to cross correlate a  
6 principal Laurent component of the inphase signal with a gate  
7 function relative to the odd modulo count of the timing signal, and  
8 the quadrature magnitude error generator generates the  
9 quadrature magnitude error signal from a difference between a  
10 filter response of the quadrature signal and an even modulo count  
11 of the timing signal, the quadrature magnitude error generator  
12 serving to cross correlate a principal Laurent component of the  
13 inphase signal with a gate function relative to the even modulo  
14 count of the timing signal.

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16 4. (Original) The symbol timing synchronizer for claim 1 wherein,  
17 inphase and quadrature serial demodulators respectively filter  
18 principal Laurent components of the inphase and quadrature signals  
19 for providing odd and even Laurent filter responses, and

20 inphase and quadrature serial demodulators respectively  
21 sample the odd and even Laurent filter responses for generating the  
22 odd and even data.

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24 5. (Original) The symbol timing synchronizer of claim 1 further  
25 comprising

26 an input sampler for sampling the received signal into the  
27 sampled input signal sampled at a rate of the timing signal.

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1 6. (Original) The symbol timing synchronizer of the claim 1 further  
2 comprising,

3 a multiplexer for multiplexing the odd and even data into the  
4 estimate of the input data sequence.

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6 7. (Original) The symbol timing synchronizer of claim 1 wherein,  
7 the received input system is a Gaussian minimum shift keying  
8 signal have a bit bandwidth product of 1/5 and a modulation index  
9 of 1/2.

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11 8. (Currently Amended) The symbol timing synchronizer of claim 3  
12 wherein,

13 the odd modulo count is  $(2k+1)N$  where  $N$  is the modulo count of  
14 the modulo counter, and

15 the even modulo count is  $(2k)N$  where  $N$  is the modulo count of  
16 the modulo counter, where  $k$  is a symbol index.

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18 9. (Currently Amended) The symbol timing synchronizer of claim 1  
19 wherein

20 the odd error signal is an  $e_{2k+1}$  odd error signal, and

21 the even error signal is an  $e_{2k}$  even error signal, where  $k$  is a  
22 symbol index.

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1 10. (Original) The symbol timing synchronizer of claim 1 further  
2 comprising

3 a carrier phase synchronizer for generating a phase adjustment  
4 signal from a sampled phase adjusted input signal and the timing  
5 signal,

6 an input mixer for adjusting the received input signal into a  
7 phase adjusted input signal, and

8 an input sampler for sampling the phase adjusted input signal  
9 into the sampled phase adjusted input signal.

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11 11. (Original) The symbol timing synchronizer of claim 10 wherein  
12 the carrier phase synchronizer comprises,

13 an inphase isolator and a quadrature isolator for respectively  
14 isolating the sampled inphase component and sampled quadrature  
15 component for providing an inphase signal and a quadrature signal,

16 an inphase serial data demodulator and a quadrature serial  
17 data demodulator for respectively receiving and filtering the  
18 inphase signal and the quadrature signal for generating an odd  
19 filter response and an even filter response, and for converting and  
20 sampling the odd and even filter responses into odd data and even  
21 data, the odd data and the even data alternately forming an  
22 estimate of the input data sequence,

23 an odd mixer and an even mixer for respectively mixing the  
24 even filter response and the odd data signal into an odd error  
25 signal and mixing the odd filter response signal and the even data  
26 signal into an even error signal, and

27 an oscillator means for converting the odd and even error  
28 signals into the phase adjustment signal.

1 12. (Original) A symbol timing synchronizer for generating a timing  
2 signal from a sampled input signal being a received input signal  
3 sampled at a rate of the timing signal, the received input signal  
4 being a continuous phase modulated signal modulated by a symbol  
5 sequence generated from a precoded data sequence of an input data  
6 sequence, sampled input signal having a sampled inphase component  
7 and a sampled quadrature component, the symbol timing synchronizer  
8 comprising,

9       an inphase isolator and a quadrature isolator for respectively  
10 isolating the sampled inphase component and sampled quadrature  
11 component of the sampled input signal for respectively providing an  
12 inphase signal and a quadrature signal,

13       an inphase early-late gate and a quadrature early-late gate  
14 for respectively filtering the inphase signal and the quadrature  
15 signal for generating an inphase gate signal and a quadrature gate  
16 signal, the inphase and quadrature early-late gates respectively  
17 serving to cross correlate the inphase and quadrature signals with  
18 gate functions in synchronism with the timing signal,

19       an inphase transformer and a quadrature transformer for  
20 respectively transforming the inphase signal and the quadrature  
21 signal for generating an inphase transformed signal and a  
22 quadrature transformed signal,

23       an inphase gate sampler and a quadrature gate sampler for  
24 respectively sampling inphase gate signal and the quadrature gate  
25 signal for generating a sampled inphase gate signal and a sampled  
26 quadrature gate signal,

27       an inphase transformer sampler and a quadrature transformer  
28 sampler for respectively sampling the inphase transformed signal

1 and the quadrature transformed signal for generating a sampled  
2 inphase transformed signal and a sampled quadrature transformed  
3 signal,

4 an inphase hard limiter and a quadrature hard limiter for  
5 respectively converting the sampled inphase transformed signal into  
6 odd data and the sampled quadrature transformed signal into even  
7 data,

8 an inphase mixer and a quadrature mixer for respectively  
9 mixing the sampled inphase gate signal and odd data into an odd  
10 error signal and mixing the sampled quadrature gate signal and even  
11 data signal into an even error signal, and

12 an oscillator means for generating the timing signal from the  
13 even error signal and the odd error signal, the oscillator means  
14 for controlling the sampling of the inphase and quadrature gate  
15 samplers and the inphase and quadrature transformer samplers for  
16 generating the timing signal at a rate of the symbol sequence.

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19 13. (Original) The symbol timing synchronizer of claim 12 wherein  
20 the oscillator means comprises,

21 a loop filter for receiving the odd error signal and the even  
22 error signal for providing a filter error signal,

23 a controlled oscillator for receiving the filter error signal  
24 for generating the timing signal, and

25 a modulo counter for providing an odd timing signal for  
26 sampling the inphase magnitude error signal, and for providing an  
27 even timing signal for sampling the quadrature magnitude error  
28 signal.

1 14. (Original) The symbol timing synchronizer of claim 12 wherein,  
2 the inphase and quadrature early-late gates function as cross  
3 correlators for cross correlating a filter response isolating  
4 principal Laurent components of the inphase and quadrature signals  
5 with a gating function,

6 the inphase gate signal is an inphase magnitude error signal  
7 from the correlation of an inphase early-late gate filter response  
8 of the inphase signal and the gating function that is in  
9 synchronism with an odd modulo count of the timing signal, and

10 the quadrature gate signal is a quadrature magnitude error  
11 signal from the correlation of a quadrature early-late gate filter  
12 response of the quadrature signal and the gating function that is  
13 in synchronism an even modulo count of the timing signal.

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15 15. (Original) The symbol timing synchronizer for claim 12 wherein,  
16 the inphase and quadrature transformers, transformer samplers  
17 and hard-limiters respectively are inphase and quadrature serial  
18 demodulators,

19 the inphase and quadrature transformer are principal Laurent  
20 component filters providing the inphase and quadrature transformed  
21 signals that respectively are odd and even Laurent filter  
22 responses, and

23 the odd and even data alternately forming an estimate of the  
24 input data sequence.

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1 16. (Original) The symbol timing synchronizer of claim 12 further  
2 comprising

3 an input sampler for sampling the received signal into the  
4 sampled input signal sampled at a rate of the timing signal, and  
5 a multiplexer for multiplexing the odd and even data into the  
6 estimate of the input data sequence.

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9 17. (Currently Amended) The symbol timing synchronizer of claim 12  
10 wherein,

11 the received input system is a Gaussian minimum shift keying  
12 signal have a bit bandwidth product of  $1/5$  and a modulation index  
13 of  $1/2$ ,

14 the odd modulo count is  $(2k+1)N$  where  $N$  is the modulo count of  
15 the modulo counter,

16 the even modulo count is  $(2k)N$  where  $N$  is the modulo count of  
17 the modulo counter,

18 the odd error signal is an  $e_{2k+1}$  odd error signal, and

19 the even error signal is an  $e_{2k}$  even error signal, where  $k$  is a  
20 symbol index.

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22 18. (Original) The symbol timing synchronizer of claim 12 further  
23 comprising

24 a carrier phase synchronizer for generating a phase adjustment  
25 signal from a sampled phase adjusted input signal and the timing  
26 signal,

27 an input mixer for adjusting the received input signal into a  
28 phase adjusted input signal, and

1        an input sampler for sampling the phase adjusted input signal  
2 into the sampled phase adjusted input signal.

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4 19. (Original) The symbol timing synchronizer of claim 18 wherein  
5 the carrier phase synchronizer comprises,

6        a carrier inphase isolator and a carrier quadrature isolator  
7 for respectively isolating the carrier sampled inphase component  
8 and carrier sampled quadrature component for providing a carrier  
9 inphase signal and a carrier quadrature signal,

10       an inphase sampler and a quadrature sampler for respectively  
11 sampling at the rate of the timing signal the carrier inphase  
12 signal and the carrier quadrature signal for providing a carrier  
13 sampled inphase signal and a carrier sampled quadrature signal,

14       a carrier inphase transformer and a carrier quadrature  
15 transformer for respectively transforming the carrier sampled  
16 inphase signal and carrier sampled quadrature signal into a carrier  
17 inphase transformed signal and a carrier quadrature transformed  
18 signal,

19       a carrier inphase hard limiter and a carrier quadrature hard  
20 limiter for respectively converting the carrier inphase transformed  
21 signal and carrier quadrature transformed signal into a carrier odd  
22 hard limited signal and a carrier even hard limited signal,

23       a carrier modulo counter for receiving the timing signal and  
24 generating a carrier odd timing signal and a carrier even timing  
25 signal,

26       a carrier odd sampler and a carrier even sampler for  
27 respectively sampling at the rate of the carrier odd and even

1 timing signals for sampling the carrier odd and even hard limited  
2 signals into carrier odd data and carrier even data,

3 a carrier odd mixer and a carrier even mixer for respecting  
4 mixing the carrier quadrature transformed signal and the carrier  
5 odd data signal into a carrier odd error signal and the carrier  
6 inphase transformed signal and the carrier even data signal into a  
7 carrier even error signal, and

8 a carrier oscillator for converting the carrier odd and even  
9 error signals into the phase adjustment signal.

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